SUB-HALF-MICRON GaAs FETs FOR APPLICATIONS THROUGH K BAND

C. Huang, A. Herbig, R. Anderson
Avantek, Inc.
3175 Bowers Avenue
Santa Clara, CA 95051

ABSTRACT

Sub-half-micron gate GaAs FETs fabricated on high quality VPE buffer material have achieved state-of-the-art low noise performances. Best noise figures of 0.58 dB at 4 GHz and 1.29 dB at 12 GHz have been observed. Power added efficiency of 35% at Ku band is also reported.

Introduction

The technology drive on GaAs FETs for the past ten years has concentrated on half-micron and sub-half-micron gate dimensions. Recently, quarter micron gate devices have been reported.[1] The microwave performances are outstanding up to 30 GHz. However, with the ever shrinking of device gate lengths, there are associated technological problems.

In this paper, we describe sub-half-micron gate FETs with gate lengths of between 0.3 and 0.4 microns. These devices alleviate some of the chronic problems associated with short dimension gate devices - such as, transconductance compression near pinch-off, high gate resistance and high parasitic source resistance. With this new approach, the device results are superior to the reported data for quarter micron gate devices.

The short gate device technology, low noise results, power results and high frequency applications will be discussed below.

Technology

The technological approaches under consideration include both material preparation and device fabrication.

Material Preparation

The active layers of the FETs are formed on high quality VPE buffer layer material. The buffer layer has an impurity concentration of less than $10^{13}cm^{-3}$ resulting in greatly enhanced conductivity and drift velocity at the active layer - buffer layer interface. Examples of typical doping density and mobility profiles are shown in Figure 1. The mobilities are measured using Pucel's FAT FET model[2] and are shown to be enhanced at the interface. At the active/buffer interface, the doping concentration profile is very abrupt (less than 200Å for a decade roll-off of doping concentration).

The combination of the abrupt doping cut-off, mobility and drift-velocity enhancement at the interface greatly improves the current control in the FET near channel pinch-off conditions. With sub-half-micron gate length and the proper active layer doping, gain bandwidth products ($f_T=gm/2\pi Cgs$) of 50 GHz have been achieved with devices biased at optimum noise figure. These data are much better than the f_T of 16 GHz reported recently for a 0.5 μm gate device.[3]

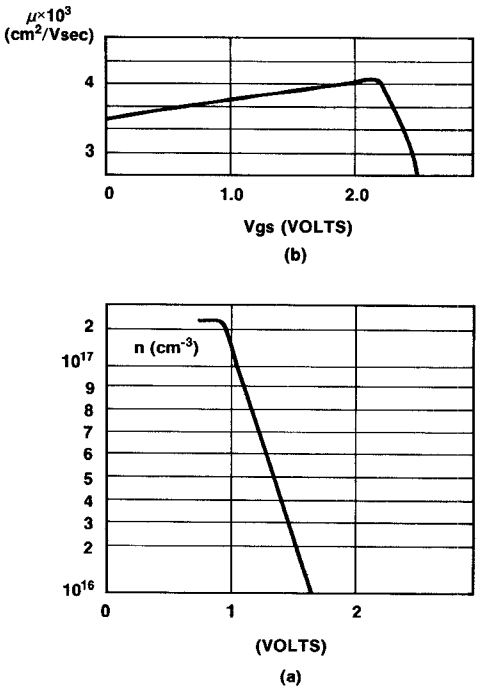

Figure 1. The doping and mobility profiles (a) doping, (b) mobility.

Effectively, the mobility and drift velocity enhancements near the active-buffer layer interface reduce transconductance compression problems. This not only improves device low noise performance but improves linear power as well. As a result, the devices have a high power added efficiency at 1-dB gain compression power out. This will be discussed later.

Device Fabrication

In Figure 2, a SEM micrograph shows the cross section of a unique gate structure. It is fabricated with a patented plated gate process.[4] The gate has an ideal trapezoidal structure that not only minimizes the resistance but also improves the device reliability. Optical lithography is used throughout to fabricate the devices.

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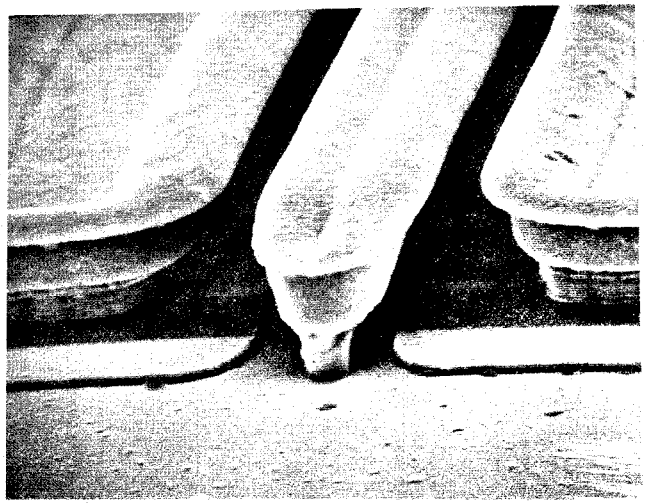


Figure 2. A typical cross section of the gate.

The gate employs a TiW/Au refractory metallization system. This system is more resistant to environmental and processing related corrosion than aluminum metallization systems. It is reliable without the need of a dielectric protection layer.[5] It is also compatible with conventional gold wire bonding operations without an intermediate barrier metal system.[6] As a result, one process step is eliminated improving the overall process yields.

A relatively large source resistance is usually a problem because of the small active layer thickness employed in the fabrication of short gate devices. This problem is solved by using multiple recess gate steps to reduce the parasitic source resistance without a correspondent increase in capacitive feedback between drain and gate. This geometry helps to improve the low noise and gain performances of sub-half-micron gate devices.

The material and device technologies described above have been used to fabricate a family of low noise and high power FETs. The results achieved to date will be summarized below.

Applications

Low Noise

Figure 3 shows the best device noise figures observed to date. The dash lines show the frequency dependence of the device noise figures and associated gains. The key results are 0.58 dB noise figure at 4 GHz with 16.6 dB associated gain and 1.29 dB noise figure at 12 GHz with 10.0 dB associated gain. These results are directly derived from the noise figure measurements without corrections for tuner losses but with corrections for second stage contributions. Single stage narrow band amplifiers have been built to confirm that the results obtained can be utilized in practical circuits.

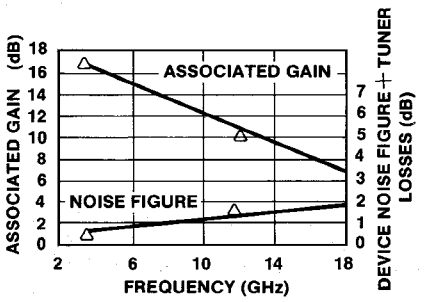
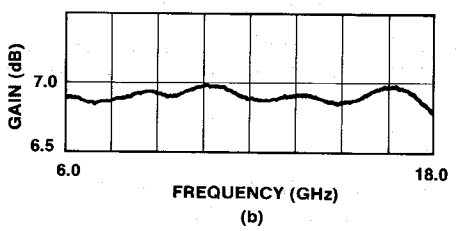


Figure 3. Best device noise figures and associated gains as a function of frequency. The noise figures measured include the tuner losses but are corrected for second stage contributions.

The applications of these low noise devices include a TVRO LNA for 3.7-4.2 GHz satellite communication band. Amplifiers with noise figures of less than 1.0 dB across the band have been fabricated. The amplifiers have isolators in the input stage which contribute to between 0.1-0.2 dB insertion loss. The total amplifier gain is 50 dB.

Other applications are 6-18 GHz broadband amplifiers. Low noise and gain modules have been fabricated with a gain of 6.5 dB per module (including the couplers). These results are shown in Figure 4.



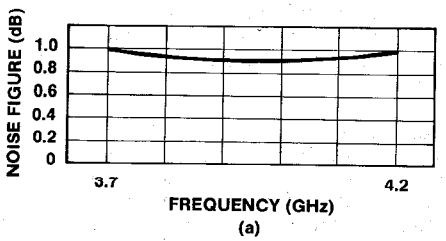


Figure 4. (a) A 1.0 dB noise figure 3.7-4.2 GHz LNA.
(b) A 6-18 GHz module with 6.5 dB gain per module.

High Power

The main difference between power FETs and low noise FETs, aside from material and design considerations, is the increased device gate width for power FETs. In Figure 5, we have shown an air bridge structure which connects the separate drain fingers of a device. The air bridge technique greatly improves the flexibility of mask layout for devices with large gate width[7] and has been shown to be very reliable.

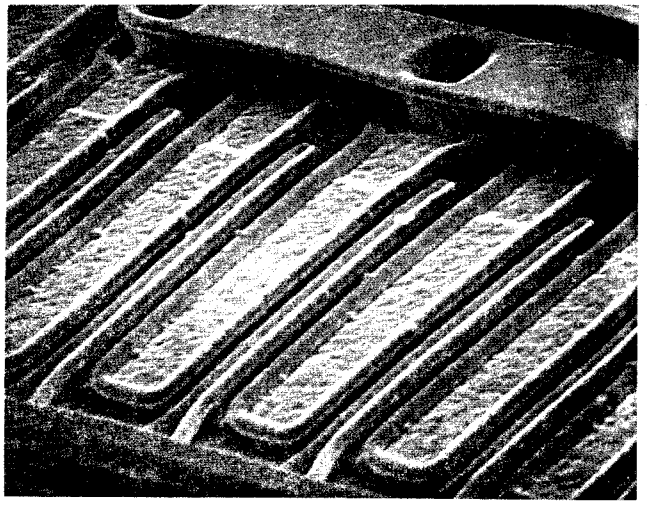


Figure 5. An air bridge structure.

The air bridge connections contribute a minimum amount of parasitic capacitances and are very useful for high frequency applications. With the short gate technologies and air bridge interconnections, a device with 2.5-mm total gate width has achieved one-watt of output power at 1-dB compression with a power added efficiency of 35% at 12 GHz.

Some of the power FET applications include five watt amplifiers at 4 GHz and 6 GHz and one-watt amplifiers at Ku band.

High Frequency

For applications at frequencies higher than 18 GHz, the major FET challenge is to have a useful gain of more than 8.0 dB. In Figure 6, a one stage amplifier demonstrates a minimum of 6.0 dB gain across the 18-26.5 GHz band using a sub-half-micron gate FET. Device applications up to 40 GHz are presently under investigation.

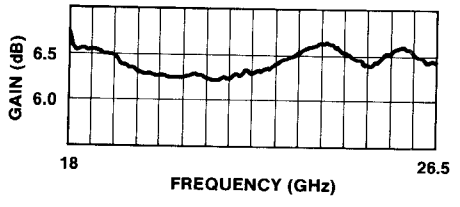


Figure 6. A 18-26.5 GHz module with 6.0 dB gain per module.

Summary

Novel sub-half-micron gate FETs with state-of-the art low noise performances have been reported. The unique technology approaches overcome some of the shortcomings of ultra-short gate FETs. Application examples have been shown. Device applications up to 40 GHz will become feasible in the near future.

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